DELAYED-LOCKED LOOP WITH FINE AND COARSE CONTROL USING CASCADED PHASE INTERPOLATOR AND VARIABLE DELAY CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to clock generation circuits for integrated circuit devices, and more particularly, to delay locked loop (DLL) circuits.

As the processing speed of electronic systems has increased, there has been increased focus on high-speed inter-chip signaling. High-speed inter-chip communication often requires precise clock signals for clocking data signals, and is often desirable that such clock signals provide such precision over a wide range of clock frequencies. Phase-locked loop (PLL) or DLL circuits are commonly used to produce such precision clock signals.

Some conventional DLL circuits use phase interpolators to provide fine phase adjustment of clock signals. For example, in some conventional approaches, a first DLL loop is used to create a plurality of quadrature clock signals. A selected pair of these quadrature clock signals is then applied to a phase interpolator loop, which generates a clock with a phase that is interpolated between the selected quadrature clocks. An exemplary dual-loop DLL circuit along these lines is described in an article by Sidiropolous and Horowitz et al. entitled "A Semi-Digital Dual Delay-Locked Loop," IEEE Journal of Solid-State Circuits, vol. 32, no. 11 (November 1997). Other dual loop circuits are described in "Pixel-Flow System Documentation: IV.9 Clock Input Buffer and Delay-Locked Loop," University of North Carolina, rev. 6.0 (Jan 23, 2001), available on the World Wide Web at www.cs.unc.edu/~msl/PadLibrary/IV.9.pdf.

Although these and other prior art DLL circuits can provide precision clock control, there is an ongoing need for DLL circuits that can provide precision phase control and wide operating range.

SUMMARY OF THE INVENTION

According to some embodiments of the present invention, a delay-locked loop (DLL) circuit comprises a phase interpolator circuit and variable delay circuit coupled in cascade and operative to generate an output clock signal that is delayed with

respect to a reference clock signal responsive to respective first and second control signals applied to the phase interpolator and the variable delay circuit. The DLL circuit further comprises a phase control circuit that generates the first and second control signals responsive to the output clock signal and the reference clock signal.

The variable delay circuit may provide a coarser resolution than the phase interpolator circuit. For example, the variable delay circuit may comprise a tapped delay chain circuit configured to provide step changes in delay responsive to the second control signal. In particular, the tapped delay chain circuit may comprise a plurality of delay circuits interconnected by a switching circuit that is operative to selectively bypass one or more of the delay circuits responsive to the second control signal. The phase control circuit may be operative to cause the phase interpolator circuit to shift between extremes of its delay range concurrent with a step change in delay through the variable delay circuit.

According to further embodiments of the present invention, the phase interpolator circuit comprises first and second delay circuit coupled in series and generating respective first and second delayed clock signals, and a phase interpolator (e.g., analog or digital) that receives the first and second delayed clock circuits and that generates a phase interpolated clock signal therefrom.

In additional embodiments of the present invention, the phase control circuit comprises a phase detector that generates an error signal responsive to a comparison of the reference clock signal to the output clock signal, and a delay control circuit that generates the first and second control signals responsive to the error signal. The delay control circuit may comprise a fine control counter circuit that increments and decrements a fine control count signal responsive to the error signal and that generates a count limit indicator signal responsive to the fine control count signal reaching one of a maximum or minimum count, and a coarse control counter circuit that increments and decrements a coarse control count signal responsive to the error signal subject to the count limit indicator signal. The phase interpolator circuit may be responsive to the fine control count signal, and the variable delay circuit may be responsive to the coarse control count signal. In further embodiments, the coarse control counter circuit is enabled responsive to assertion of the count limit indicator signals. The error signal may comprise first and second error signals, and the fine and coarse control counter circuits may increment and decrement responsive to respective ones of the first and second error signals.

According to further aspects of the present invention, a DLL circuit includes a cascade combination of a phase interpolator circuit and a tapped delay chain circuit. The cascade combination is operative to produce an output clock signal that is delayed with respect to a reference clock signal responsive to a control input. A phase control circuit generates the control input responsive to a comparison of the output clock signal to the reference clock signal. The phase interpolator circuit may be configured to provide a fine delay adjustment and the tapped delay chain may be configured to provide a coarse delay adjustment. The tapped delay chain circuit may comprise a cascade of selectively bypassable fixed delay circuits. A resolution of the tapped delay chain circuit may be substantially the same as a range of the phase interpolator circuit.

Related methods of operating a DLL are also described.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a DLL circuit according to some embodiments of the present invention.

FIG. 2 is a schematic diagram of a DLL circuit according to further embodiments of the present invention.

FIG. 3 is a schematic diagram illustrating a phase interpolator according to some embodiments of the present invention.

FIG. 4 is a schematic diagram illustrating a delay control circuit according to further embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Specific exemplary embodiments of the invention now will be described with reference to the accompanying drawings. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, like numbers refer to like elements. It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present.

FIG. 1 illustrates a DLL circuit 100 according to some embodiments of the present invention. The DLL circuit 100 has a single closed loop architecture having a forward path including a cascaded combination 110 of a phase interpolator circuit 112 and a variable delay circuit 114. The cascaded combination 110 produces an output clock signal 115 that is variably delayed with respect to a reference clock signal 105 responsive to a control input 125 produced by a phase control circuit 120. For example, the phase control circuit 120 may generate the control input 125 responsive to a comparison of the output clock signal 115 to the reference clock signal 105.

According to some embodiments of the present invention, the phase interpolator 112 is configured to provide fine delay control for the output clock signal 115, while the variable delay circuit 114 is configured to provide a coarse delay control for the output clock signal 115. It will be appreciated that the phase interpolator circuit 112 and the variable delay circuit 114 can be arranged in reverse order to that shown in FIG. 1, i.e., the variable delay circuit 114 may precede the phase interpolator circuit 112 in the cascade combination 110.

According to some embodiments of the present invention, it is preferable that the fine adjustment phase interpolator circuit 112 precedes the coarse adjusting variable delay circuit 114. In particular, if the fine tuning phase interpolator circuit 112 is located after the coarse tuning variable delay circuit 114, it is possible that an edge of the output clock signal 115 could receive a coarse update without a corresponding fine update, or vice versa. This could result in a large jitter or duty cycle change in the output clock signal 115, depending on which clock signal edge is affected. Although this could be avoided by requiring that no more than one clock signal edge is in the variable delay circuit 114 at any given time, this could limit the total delay through the DLL circuit 100 to within around one clock signal period. By placing the fine tuning stage before the coarse tuning stage, however, it can be ensured that each clock edge has corresponding fine and coarse tuning updates, which can allow the delay through the DLL circuit 100 to substantially exceed one clock cycle without the jitter/duty cycle phenomenon described above.

FIG. 2 illustrates a DLL circuit 200 according to further embodiments of the present invention. The DLL circuit 200 includes a phase interpolator circuit 210 including first and second cascaded delay circuits 212, 214 that generate first and second delayed clock signals 213, 215 from a reference clock signal 205. The phase interpolator circuit 210 further includes a phase interpolator 216 that receives the first

and second delayed clock signals 213, 215 and that generates a phase interpolated clock signal 217 that is phase interpolated between the first and second clock delayed signals 213, 215. The phase interpolation is governed by a first control signal 219 generated by a phase control circuit 230.

The DLL circuit 200 further includes a variable delay circuit in the form of a tapped delay chain circuit 220 that receives the phase interpolated clock signal 217 and that generates an output clock signal 225 therefrom that is variably delay responsive to a second control signal 229. As shown, the tapped delay chain circuit 220 includes a plurality of fixed delay circuits 222_1-222_n that are interconnected by a switching circuit that is operative to selectively bypass selected ones of the fixed delay circuits 222_1-222_n. In particular, the switching circuit includes multiplexers 224_1-224_{n-1} that are operative to selectively bypass selected ones of the fixed delay circuits 222_1-222_n responsive to the second control signal 229 generated by the phase control circuit 230. It will be appreciated that the second control signal 229 may comprise, for example, a count signal such as that generated by the coarse control counter circuit 428 described below with reference to FIG. 4.

As further shown in FIG. 2, the phase control circuit 230 includes a phase detector circuit 232 that generates an error signal 233 responsive to a comparison of the reference clock signal 205 and the output clock signal 225. The phase control circuit 230 further includes a delay control circuit 234 that generates the first and second control signals 219, 229 responsive to the error signal 233.

It will be appreciated that various components of the DLL circuit 200 can be implemented in a number of different ways. For example, the phase interpolator 216 may comprise an analog or digital phase interpolator. The control signals 219, 229 may be analog or digital control signals. The delay control circuit 234 may include filtering/hysteresis circuitry. The phase interpolator circuit 210 and the tapped delay chain circuit 220 may be arranged in reverse order to that shown in FIG. 2, i.e., the tapped delay chain circuit 220 may be precede the phase interpolator circuit 210 in the forward portion of the DLL loop.

FIG. 3 illustrates an exemplary analog phase interpolator 300 that may be used with the present invention. The phase interpolator 300 includes a mixer circuit 310 including first and second branches 310a, 310b that are coupled to a load 320. The respective branches 310a, 310b include respective switches 312a, 312b that operate responsive to respective ones of first and second clock signals CLK1, CLK2 that

define the range for phase interpolation (e.g., clock signals corresponding to the clock signals 213, 215 of FIG. 2). The branches 310a, 310b also include respective variable current sources 314a, 314b that are controlled by digital control signals CS1, CS2 that set tail currents and the amount of mixing by the mixer circuit 310 to control the phase of an output clock signal OLCK. For example, the control signals CS1, CS2 may be derived from a count signal generated by a counter-based control circuit, such as the fine control counter circuit 424 described below with reference to FIG. 4.

FIG. 4 illustrates an exemplary control circuit 400 according to some embodiments of the present invention. The control circuit 400 includes a phase detector circuit 410 configured to generate error signals UP, DN responsive to comparison of a reference clock signal REFCLK and a feedback clock signal FCLK (e.g., the output clock signals 115 of FIG. 1 or the output clock signal 225 of FIG. 2). The control circuit 400 further includes a delay control circuit 420 that receives error signals UP, DN from the phase detector circuit 410. As shown, the delay control circuit 420 includes a filter counter circuit 422 that counts up or down responsive to the error signals UP, DN, thus producing filtered counter command signals INC, DEC. The delay control circuit 420 also includes a fine control counter circuit 424 and a coarse control counter circuit 428 that generate fine and coarse control count signals FINE, COARSE that may be used to control fine and coarse delay control elements in a DLL responsive to the filtered counter command signals INC, DEC.

In particular, the counter command signals INC, DEC are used to increment/decrement the fine control counter circuit 424 and the coarse control counter circuit 428. The fine control counter circuit 424 generates the fine control count signal FINE, which may be used to control a phase interpolator, such as the phase interpolator 300 of FIG. 3. The fine control counter circuit 424 also generates fine control count limit indicator signals FMAX, FMIN that indicate when the fine control count signal FINE has reached respective maximum and minimum values.

The coarse control counter circuit 428 increments/decrements the coarse control count signal COARSE (e.g., a signal that may be used to control a coarse delay circuit, such as the tapped delay chain circuit 220 of FIG. 2) responsive to the counter command signals INC, DEC subject the fine control count limit indicator signals FMIN, FMAX. In particular, AND gates 426a, 426b logically combine the counter command signals INC, DEC and the fine control count limit indicator signals FMIN, FMAX such that the coarse control counter circuit 428 is not enabled (does

not increment/decrement) unless the corresponding one of the fine control count limit indicator signals FMAX, FMIN is also asserted. The meeting of such logical conditions may also cause a corresponding setting/resetting of the fine control counter circuit 424, i.e., by the application of the outputs of the AND gates 426a, 426b to set and reset S, R inputs of the fine control counter circuit 424, such that the fine control count signal FINE moves between extremes of its delay range in concert with the incrementing/decrementing of the coarse control counter circuit 428.

More particularly, when the fine control count signal FINE and the coarse count control signal COARSE are applied in a DLL circuit, such as the DLL circuit 200 of FIG. 2, to control fine and coarse delay adjustment, respectively, the coarse control count signal COARSE does not change, e.g., cause a step increase/decrease in delay through tapped delay chain circuit 220, until the fine control count signal FINE has hit a limit, corresponding to a boundary of the range of fine delay control afforded by the phase interpolator. When such a step change does occur, the fine control count signal FINE preferably is shifted in a complementary fashion to limit overcompensation, with the range of delay provided by the fine control count signal FINE preferably being substantially the same as the delay resolution provided by the coarse control count signal COARSE. Oscillation between delay step changes produced by the coarse control count signal COARSE can be damped by the action (hysteresis) provided by the filter counter circuit 422. In this manner, a smooth interaction of fine and coarse delay adjustment can be achieved.

In the drawings and specification, there have been disclosed exemplary embodiments of the invention. Although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being defined by the following claims.